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(54) **A process of linearizing non-linear analog-to-digital conversion the process and circuit for performing.**

(57) A circuit for linearizing analog-to-digital output is shown in Figure 2, with an analog signal V_i transmitted by input circuit 10 is applied to an input port of an analog-to-digital converter 12 controlled by a sampling signal V_s, to provide digital data V_d on an "N" bit data bus 14. An analog-to-digital linearizing memory 16 storing a look-up table of digital values, is coupled to bus 14 to receive the digital data V_d, and to respond to the digital data V_d by providing true linear digital values from the look-up table to digital data processing system DSP 20 via an "N" bit data bus 18. A microprocessor 22 is temporarily coupled between the output port of converter 12 and the input port of memory 16 via bus 14, to serve as a switch between bus 14 and a programming memory 24 containing a table of true linear digital values V_t. A known test signal is applied to input circuit 10, and true linear digital values V_t stored in programming memory 24, are then read into linearizing memory 16 to provide an accurate and reliable relation to a characteristic such as the amplitude of each step of the known test signal over the entire range of the known test signal.

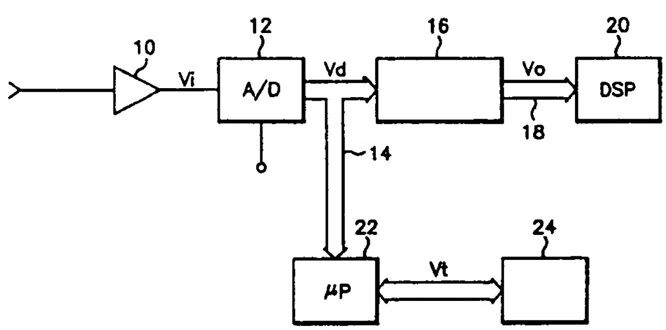

FIG. 2

EP 0 514 587 A2

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Field of the Invention

The current invention relates to processing of digital signals and, more particularly, to processes and circuits for converting analog signals into digital representations of those analog signals.

Background

Digital signal processing (DSP) systems usually have an A/D converter as an input link from the analog domain. An analog-to-digital (i.e., an "A/D") converter is always assumed to provide a digital signal based on the input level. For a given peak-to-peak input of V_{pp}, an A/D converter generates a given number of codes at its output port. Consequently, the input-to-output linearity of an A/D converter is very important.

Currently available high priced A/D converters have one or more linearity controls. These controls allow the user to adjust the output for a given input (e.g., either 50%, or 25% and 75%) level to obtain a linear output. Frequently however, there is some non-linearity in the intermediate input levels.

For commercial grades of consumer appliances using mass production quality analog-to-digital converters such as video signal products, it is imperative that the degree of non-linearity of the analog-to-digital converter be kept under control. For example, in deghoster circuits, the ghost parameters may be computed from a transition in a given region; by way of illustration, a vertical synchronization signal (-40 to 0 IRE) or 0 → 70 IRE broadcast television (i.e., a BTA) signal. Then, the entire -40 to ≈ 120 IRE video signal is "deghosted" based on these parameters. Thus, for reliable deghosting performance, the "assumed" linearity of the signal is extremely important.

Earlier efforts by others to obtain particular output characteristics from analog-to-digital converters have tended toward two different approaches. One approach used an expensive, high-quality analog-to-digital converter designed to include adjustable gain and phase stages. Prior to use, each of the adjustable stages would necessarily be "tuned" to give optimal output characteristics. Cost of the converter, and the time consumed in making the adjustments, are two problems attendant to the first approach. Consequently, the use of such converters is limited to customized, expensive applications.

The second approach, as represented by Kimura, U.S. Patent No. 4,764,751, applies the output signal "z" from a non-linear analog-to-digital conversion circuit to a look-up table memory containing straight line conversion data, in an effort to obtain compensated digital values "z'" stored the look-up table, and to thereby provide a conversion exhibiting a particular non-linear (e.g., logarithmic) characteristic. Several stages are coupled to the input port of the non-linear analog-to-digital conversion circuit to adjust offset and gain of the analog signals being applied to the conversion circuit. This approach however, requires measurement of conversion characteristic data of the non-linear analog-to-digital converter, calibration of the conversion characteristic data curve at an origin and at the maximum output value (e.g., 2^N-1) as part of a normalization and curve-fitting step, and calculation of compensated digital values corresponding to the level of the input signal in terms of reference data and the conversion characteristic data. Consequently, because this approach necessarily demands reliance upon offset and gain adjustment stages, the use of specialized digital-to-analog converters, and measurement of the conversion characteristic data of the converters, it is unsuitable for use with mass production quality analog-to-digital converters. Moreover, this approach neither recognizes, nor addresses the problem of improving the linearity of conversion by linear digital-to-analog converters at values intermediate to the two extremes of the range of conversion.

Summary of the Invention

Accordingly, it is one object of the currently disclosed invention to provide an improved process and circuit for performing digital to analog conversion.

It is another object to provide a process and circuit exhibiting an enhanced degree of linearity in conversion of analog signals to digital signals.

It is still another object to provide a process and circuit suitable for inexpensively correcting deviations in the linearity of mass produced analog-to-digital converters.

It is yet another object to provide a process and circuit characterized by an enhanced input to output linearity of digital to analog conversion independently of offset, gain and phase adjustments.

These and other objects are achieved with a process and circuit using a memory storing linearizing data values interposed between an analog-to-digital converter and a digital signal processing system. A known analog test signal such as a ten step IRE staircase, is incrementally applied to an input port of the digital-to-analog converter while a programming stage applies digital values for the known analog signal amplitudes to the memory at each of the steps to assure coincidence between the provisional digital signal generated by the analog-to-digital converter and the corresponding addresses of the linear digital values stored within the memory. Once corresponding addresses for the linear digital values are stored within the mem-

ory, the programming stage is removed and the serially coupled analog-to-digital converter and memory will reliably provide a greater degree of linearity between the analog signals applied to the converter and the digital values emanating from the memory.

Brief Description of the Drawings

A more complete appreciation of the inventions, and many of the attendant advantages thereof, will be readily enjoyed as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like numbers indicate the same or similar components, wherein:

Figure 1 is a schematic block diagram of a conventional application of an analog-to-digital converter.

Figure 2 is a schematic block diagram of an analog-to-digital converter circuit constructed according to the principles of the currently disclosed invention.

Figure 3 is a graphical representation of a ten step IRE staircase signal.

Figure 4 is a two coordinate graphical illustration of deviations in the degree of linearity occurring in a representative commercially available analog-to-digital converter.

Figure 5 is a two coordinate graphical illustration of one implementation of a process for performing analog-to-digital conversion according to the principles of the currently disclosed invention.

Figure 6 is a two coordinate graphical illustration of actual and theoretical responses obtained with one embodiments constructed according to the principles of the currently disclosed invention.

Figures 7A, 7B and 7C are two coordinate graphical illustrations providing expanded presentation of the detail of adjoining sections of the values illustrated in the graphical representation of Figure 6.

Detailed Description of the Invention

Referring now to Figure 1, a schematic illustration of a representative conventional digital signal processing system is shown. Such systems usually have an analog-to-digital converter as an input link from the analog domain. In the system of Figure 1, an analog signal is applied to an input port of an input circuit 10 which includes a gain adjustment stage, a direct current offset adjustment stage, and a clamp. The analog clock V_c transmitted by input circuit 10 is applied to an input port of an analog-to-digital converter 12 controlled by a sampling clock V_c, to provide digital data V_d on an "N" bit data bus 14 to a digital data processing system DSP 20. Referring now to Figure 4, a comparison of the uncorrected digital data V_d generated by converter 12 against the straight-line labelled "true linear A/D converter output, shows that the digital data V_d deviates almost continuously over the range of conversion of converter 12, from a desired true linear relation between the A/D input analog signal V_i applied to the input port of converter 12 and the digital data V_d generated by converter 12.

A very simple circuit for linearizing analog-to-digital output according to the principles of the current inventions, is illustrated in Figure 2. As was shown in Figure 1, the analog signal V_i transmitted by input circuit 10 is applied to an input port of an analog-to-digital converter 12 controlled by a sampling clock signal V_c, to provide digital data V_d on an "N" bit data bus 14.

An analog-to-digital linearizing memory 16, such as, for example, a programmable read-only-memory (i.e., a "PROM") storing a look-up table of digital values, is coupled to bus 14 to receive the digital data V_d, and to respond to the digital data V_d by providing true linear digital values from the look-up table to digital data processing system DSP 20 via an "N" bit data bus 18.

A microprocessor 22 may be temporarily coupled between the output port of converter 12 and the input port of memory 16 via bus 14, to serve as a switch between bus 14 and a programming memory 24 containing a table of true linear digital values V_t.

A known test signal such as a ten step IRE staircase signal, as shown in Figure 3, may be used as the analog input signal applied to input circuit 10. In such an instance, the true linear digital values V_t stored in programming memory 24 provide an accurate and reliable relation to a characteristic such as the amplitude of each step of the known test signal over the entire range of the known test signal. An IRE zone shown along the abscissa of the graph in Figure 3, is defined as an output range between the levels captured from the test signal. A, and B are analog-to-digital output values defining the Kth zone for input level or interval V_k to V_{k+1}. A_T, an B_T are corresponding correct (true linear) values for that zone. Then, a corrected value Y_T for the digital value Y of the non-linear A/D may be computed as:

$$Y_T = A_T + [(B_T - A_T)] * [(y-A) \div (B-A)] \quad (1)$$

$$= [A_T - [(B_T - A_T) \div (B-A)] * A] + [(B_T - A_T) \div (B-A)] * y \quad (2)$$

$$= C_k + D_k * y \quad (3)$$

where C_k and D_k are the parameters computed for the K_{th} zone from its measured values of A and B for a given A/D device with corresponding theoretical analog-to-digital output values of A_T and B_T.

The analog-to-digital output that results from a known test signal such as a ten step IRE staircase signal, is gated to microprocessor 22, for example, for a nine bit analog-to-digital converter 12, after basic gain and direct current offset are adjusted within input circuit 10 for a 0 to +1 V_{pp} signal input. The analog-to-digital output digital value will therefore range by 2^N, with $N = 9$, from -256 to +255 in offset two's complement. Microprocessor 22 obtains true digital values V_t from the look-up table stored within programming memory 24, for the known IRE levels. Correct digital values for each of these levels of amplitude of the IRE staircase test signal are known for the designated analog-to-digital device, and are stored within a look-up table within programming memory 24. In response to application of each of the levels of the IRE staircase test signal to input circuit 10, microprocessor 22 reads the corresponding true digital value V_t from programming memory 24 and stores that true digital value within the look-up table of linearizing memory 16, the corresponding true digital value, with the address of each of the true digital values stored within linearizing memory 16 being the corresponding uncorrected digital data V_d generated by converter 12. A microprocessor 22 is programmed to determine values between steps of an input signal analytically, as shown in Figure 5 for the step of V_k to V_{k+1}. After all of the true digital values over the range of converter 12 are stored within the look-up table of linearizing memory 16 at address corresponding to the values of digital data V_d generated by converter 12 in response to input of each of the levels of the known test signal, microprocessor 22 and programming memory 24 are removed and a linear analog-to-digital converter including input circuit 10, converter 12 and linearizing memory 16 are able to accurately generate digital values V_o exhibiting a true linear relation with a characteristic, such as amplitude, of an input analog signal V_I, over the entire range of converter 12. Thus, the input-to-output non-linearity intrinsic to a mass production quality analog-to-digital converter 12 can be reliably and inexpensively eliminated, or greatly reduced, simply by generating appropriate mapping via a read only memory (i.e., a "ROM") 16.

The plots illustrated in Figures 6, 7A, 7B and 7C were made for a TRW nine bit analog-to-digital converter evaluation board, Model No. TDC 1020 E1C. Figure 6 provides a two coordinate graphical illustration of actual and theoretical responses obtained with one embodiments constructed according to the foregoing principles currently disclosed, while figures 7A, 7B and 7C shown enlarged two coordinate graphical illustrations providing expanded presentation of the detail of adjoining sections of the values illustrated in the graphical representation of Figure 6. The plots of Figures 6, 7A, 7B and 7C show analog-to-digital output V_o (as dashed lines) and corrected values (as solid lines) using above described concept. The expanded views clearly depict that the nonlinearity can be practically eliminated over the entire digitizing range.

Claims

1. An analog-to-digital converter, comprising:

   means for converting amplitudes of a plurality of corresponding successive intervals of an analog signal into first digital values representative of said successive intervals of said analog signal; and

   means for storing a plurality of second digital values at different corresponding ones of a plurality of distinct addresses, said plurality of distinct addresses corresponding to specific ones of said plurality of first digital values, said plurality of second digital values extending over a range and exhibiting a linear relation over said range to said amplitudes of said analog signal, and for responding to reception of said first digital values by addressing said linear values stored at corresponding ones of said plurality of distinct address.

2. The converter of claim 1, further comprised of:

   means for providing said plurality of second digital values; and

   means connectable between said converting means and said storing means, for responding to application of a test signal exhibiting known values of said amplitudes to said converting means as said analog signal, by reading said plurality of second digital values into said storage means at addresses corresponding to said first digital values.

3. An analog-to-digital converter, comprising:

   means for converting a characteristic of a plurality of successive intervals of an analog signal into first digital values representative of said successive intervals of said analog signal; and

   means coupled to said converting means to receive said first digital values, for storing a plurality of second digital values at different corresponding ones of a plurality of distinct addresses, said plurality of second digital values extending over a range and exhibiting a linear relation over said range to said characteristic of said analog signal, and for re-

sponding to reception of said first digital values by providing said linear values stored at corresponding ones of said plurality of distinct address.

4. The converter of claim 3, further comprised of:
means for providing said plurality of second digital values; and
means connectable between said converting means and said storing means, for responding to application of a test signal exhibiting known values of said characteristic to said converting means as said analog signal, by reading said plurality of second digital values into said storage means at addresses corresponding to said first digital values.

5. The converter of claim 3, further comprised of said converting means operating upon amplitude of said analog signal as said characteristic, by converting said amplitude into said first digital values.

6. The converter of claim 4, further comprised of said converting means operating upon amplitude of said analog signal as said characteristic, by converting said amplitude into said first digital values.

7. A process for converting analog signals into digital signals, comprising:
converting a characteristic of a plurality of successive intervals of analog signal into first digital values representative of said successive intervals of said analog signal; and
storing a plurality of second digital values at different corresponding ones of a plurality of distinct addresses, said plurality of second digital values extending over a range and exhibiting a linear relation over said range of said characteristics of said analog signal; and
responding to reception of said first digital values by providing as output digital signals, said linear values stored at corresponding ones of said plurality of distinct address.

8. The process of claim 7, further comprised of:
providing said plurality of second digital values; and
responding to application of a test signal exhibiting known values of said characteristic to said converting means as said analog signal, by reading said plurality of second digital values into said storage means at addresses corresponding to said first digital values.

9. The process of claim 7, further comprised of operating upon amplitude of said analog signal as said characteristic, by converting said amplitude into said first digital values.

10. The process of claim 8, further comprised of said converting means operating upon amplitude of said analog signal as said characteristic, by converting said amplitude into said first digital values.

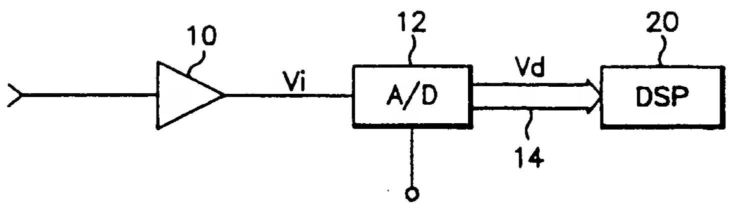


FIG. 1

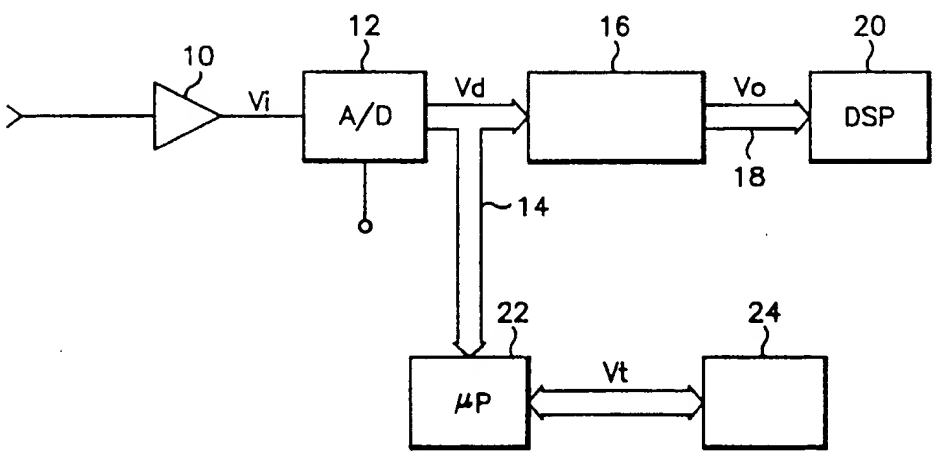
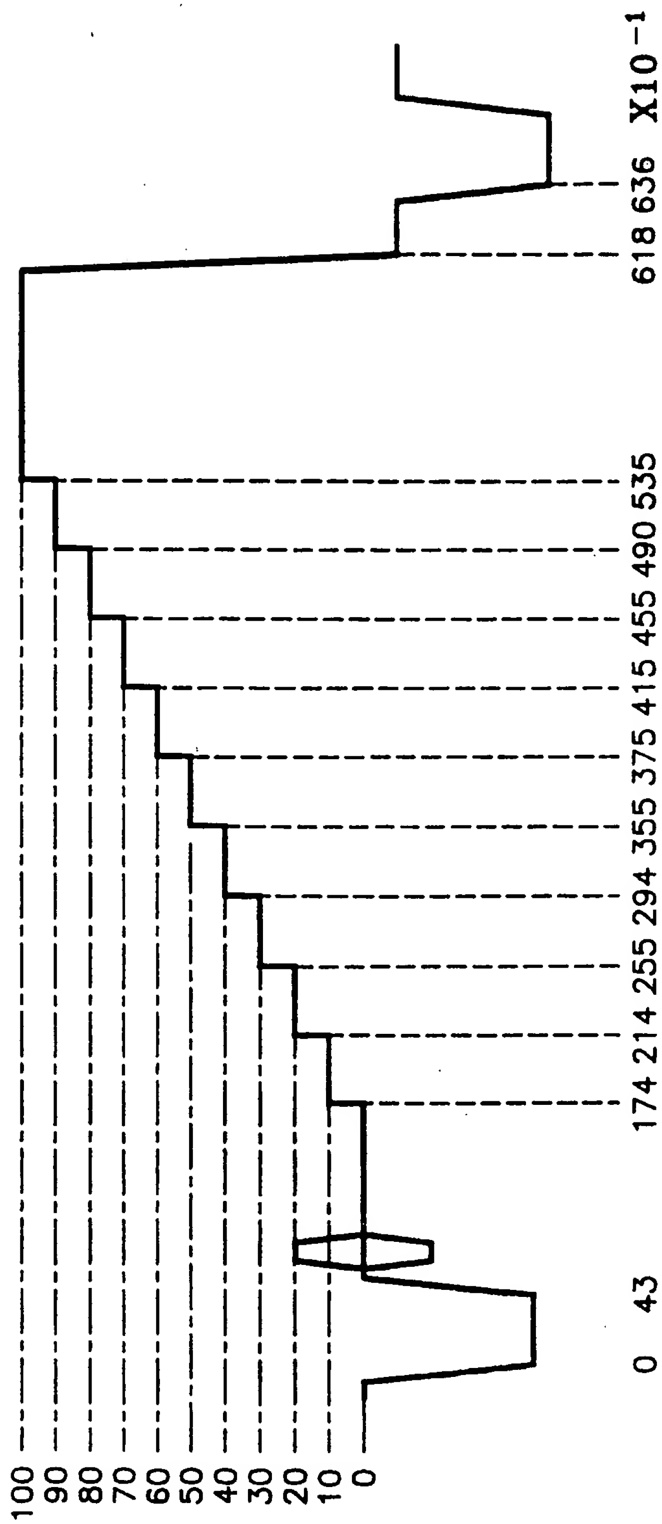


FIG. 2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60
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40
30
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618
636
X10 −1

FIG. 3

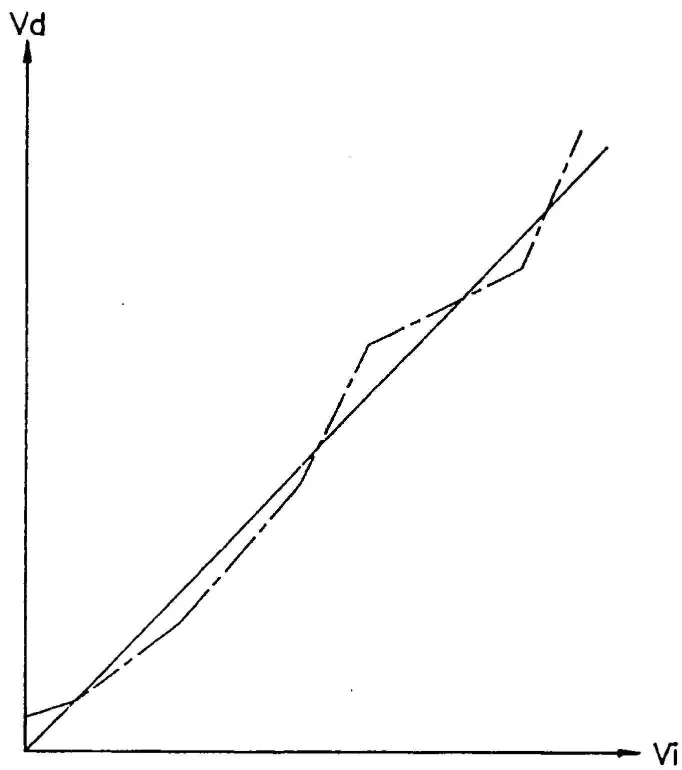
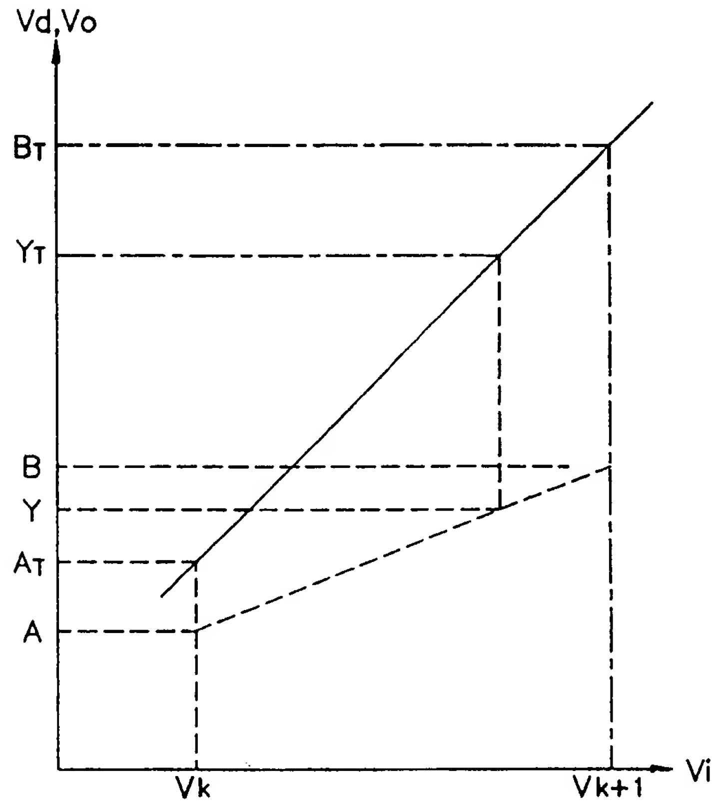
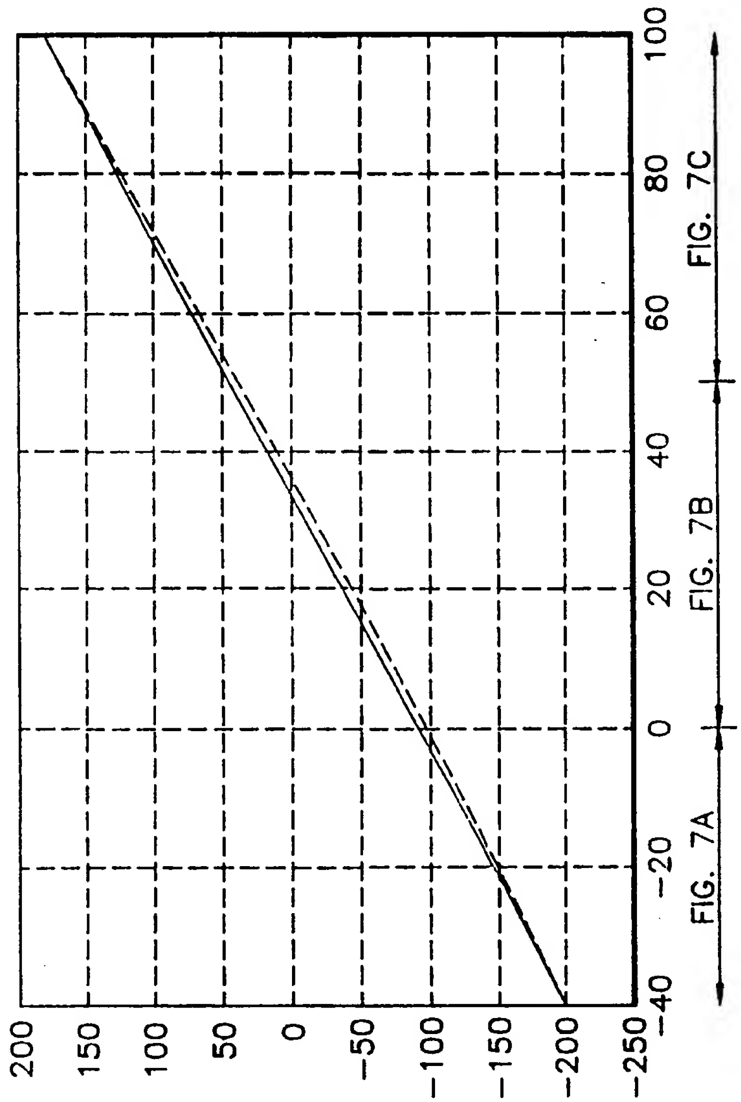


FIG. 4



$$Y_T = A_T + \frac{(Y-A)}{(B-A)} \cdot (B_T - A_T)$$

FIG. 5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−50
−100
−150
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−40
−20
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20
40
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80
100
FIG. 7A
FIG. 7B
FIG. 7C

FIG. 6

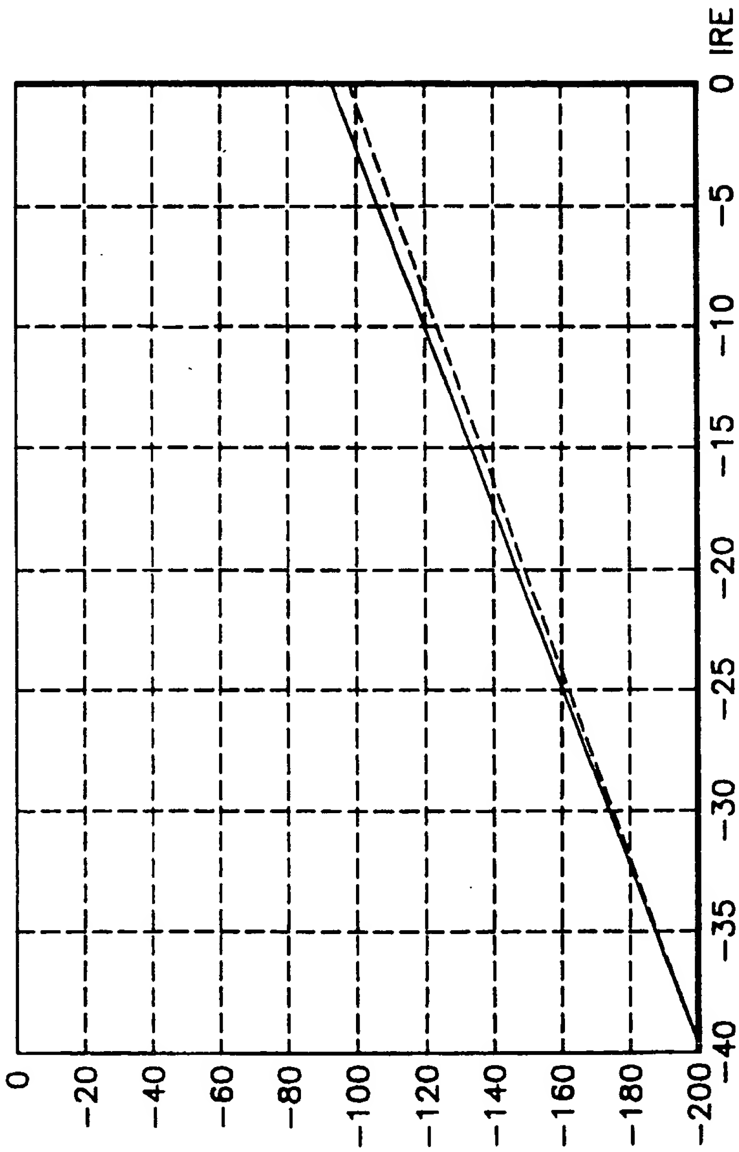

FIG. 7A

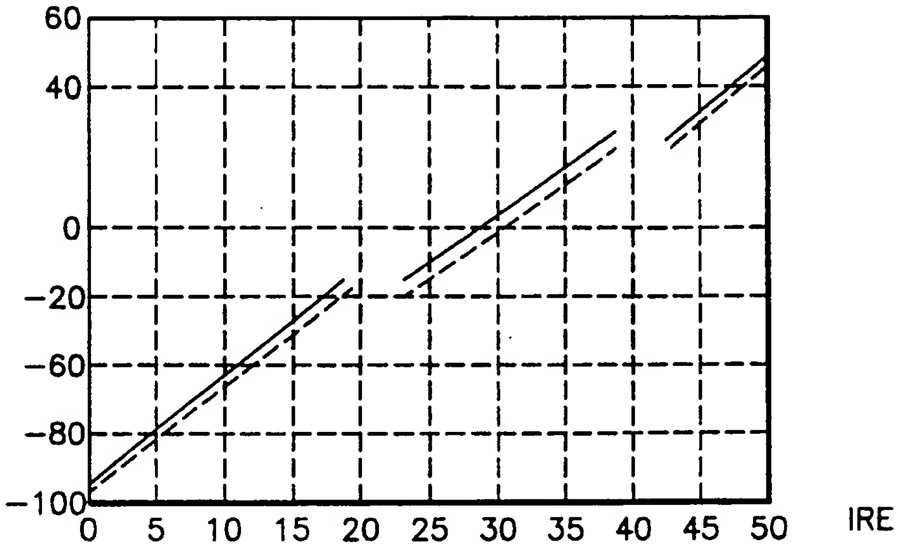
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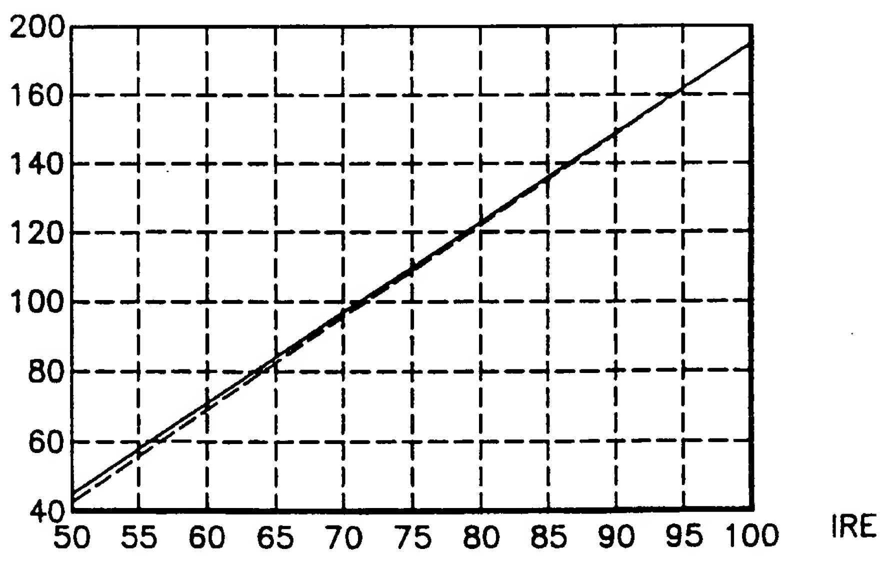
FIG. 7B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120
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50 55 60 65 70 75 80 85 90 95 100
IRE

FIG. 7C

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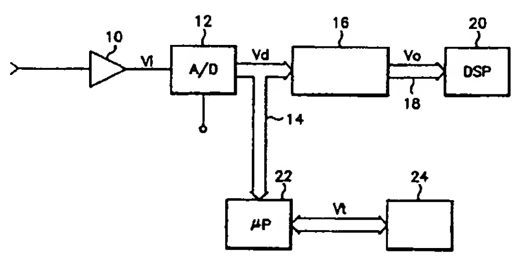

FIG. 2

EP 0 514 587 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 11 9382

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 986 243 (WEISSLER) * column 4, line 3 - column 4, line 44 * * column 8, line 12 - column 8, line 53; figures 3-4 * ---	1,3-4,7	H03M1/06
D,A	EP-A-0 231 950 (FUJIPHOTO) * claims 1,5-6 * ---	1-2	
A	FR-A-2 427 013 (SOCIETE POUR L'ETUDE ET LA FABRICATION DE CIRCUITS INTEGRES SPECIAUX) * page 6, line 10 - page 7, line 9; figure 3 * ---	1-2	
X	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS vol. 37, no. 6, June 1990, NEW YORK pages 729 - 737 , XP000149008 DENT ET AL 'Linearization of Analog-to-Digital Converters' * page 729, column 2, paragraph II - page 731, column 1, line 3; figure 2 * -----	1-2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H03M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 JULY 1993	GUIVOL Y.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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(54) A process of linearizing non-linear analog-to-digital conversion the process and circuit for performing

Verfahren zur Linearisierung einer nichtlinearen Analog-Digitalwandlung und Schaltung zur Durchführung des Verfahrens

Processus de linéarisation de conversion analogique-numérique non-linéaire et circuit de mise en oeuvre du processus

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(30) Priority: 24.05.1991 US 704986

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FR-A- 2 427 013
US-A- 4 986 243

- IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS vol. 37, no. 6, June 1990, NEW YORK pages 729 - 737 , XP000149008 DENT ET AL 'Linearization of Analog-to-Digital Converters'

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Description

Field of the Invention

[0001] The current invention relates to processing of digital signals and, more particularly, to processes and circuits for converting analog signals into digital representations of those analog signals.

Background

[0002] Digital signal processing (DSP) systems usually have an A/D converter as an input link from the analog domain. An analog-to-digital (i.e., an "A/D") converter is always assumed to provide a digital signal based on the input level. For a given peak-to-peak input of V_{pp}, an A/D converter generates a given number of codes at its output port. Consequently, the input-to-output linearity of an A/D converter is very important.

[0003] Currently available high priced A/D converters have one or more linearity controls. These controls allow the user to adjust the output for a given input (e.g., either 50%, or 25% and 75%) level to obtain a linear output. Frequently however, there is some non-linearity in the intermediate input levels.

[0004] From US-A-4 986 243 an internal combustion engine control system is known, in which an electronic circuit accepts a non-linear analogue signal from a mass air flow sensor and - digital converter. The digital signal is then processed by a two-dimensional look-up table, which includes corrections for the sensor non-linearity and additional corrections for non-linearity of the analogue-to-digital converter. This linearised signal is then used for the control of the engine.

[0005] From IEEE Transactions on Circuits and Systems, volume 37, number 6, June 1990, pages 729-737, a signal processing technique called threshold tracking is known, by which the linearity of any analogue to digital conversion circuit may be improved.

[0006] The basic principle of this technique is to use a mapping of original output codes of an analogue-to-digital converter and their associated non-ideal quantisation levels to a set of codes with corresponding quantisation levels that match more closely those of an ideal analogue to digital converter. Thereby, the error between the actual and ideal quantisation levels is reduced.

[0007] For commercial grades of consumer appliances using mass production quality analog-to-digital converters such as video signal products, it is imperative that the degree of non-linearity of the analog-to-digital converter be kept under control. For example, in deghoster circuits, the ghost parameters may be computed from a transition in a given region; by way of illustration, a vertical synchronization signal, -40 to O IRE or 0 → 70 IRE broadcast television (i.e., a BTA) signal. Then, the entire -40 to ≈ 120 IRE video signal is "deghosted" based on these parameters. Thus, for reliable deghosting performance, the "assumed" linearity of the signal is extremely important.

[0008] Earlier efforts by others to obtain particular output characteristics from analog-to-digital converters have tended toward two different approaches. One approach used an expensive, high-quality analog-to-digital converter designed to include adjustable gain and phase stages. Prior to use, each of the adjustable stages would necessarily be "tuned" to give optimal output characteristics. Cost of the converter, and the time consumed in making the adjustments, are two problems attendant to the first approach. Consequently, the use of such converters is limited to customized, expensive applications.

[0009] The second approach, as represented by Kimura, U.S. Patent No. 4,764,751, applies the output signal "z" from a non-linear analog-to-digital conversion circuit to a look-up table memory containing straight line conversion data, in an effort to obtain compensated digital values "z'" stored the look-up table, and to thereby provide a conversion exhibiting a particular non-linear (e.g., logarithmic) characteristic. Several stages are coupled to the input port of the non-linear analog-to-digital conversion circuit to adjust offset and gain of the analog signals being applied to the conversion circuit. This approach however, requires measurement of conversion characteristic data of the non-linear analog-to-digital converter, calibration of the conversion characteristic data curve at an origin and at the maximum output value (e.g., 2^N-1) as part of a normalization and curve-fitting step, and calculation of compensated digital values corresponding to the level of the input signal in terms of reference data and the conversion characteristic data. Consequently, because this approach necessarily demands reliance upon offset and gain adjustment stages, the use of specialized digital-to-analog converters, and measurement of the conversion characteristic data of the converters, it is unsuitable for use with mass production quality analog-to-digital converters. Moreover, this approach neither recognizes, nor addresses the problem of improving the linearity of conversion by linear analog-to-digital converters at values intermediate to the two extremes of the range of conversion.

Summary of the Invention

[0010] Accordingly, it is the object of the invention to provide an improved circuit and method for performing analog

to digital conversion having an enhanced degree of linearity in conversion of analog signals to digital signals and is suitable for inexpensively correcting deviations in the linearity of mass produced analog-to-digital converters independently of offset, gain and phase adjustments.

[0011] These and other objects are achieved with a converter and a method as set forth in claims 1 and 3, respectively. A preferred embodiment of the converter is subject matter of claim 2. According to the invention, a known analog test signal such as a ten step IRE staircase, is incrementally applied to an input port of the analog-to-digital converter while a programming stage applies digital values for the known analog signal amplitudes to the memory at each of the steps to assure coincidence between the provisional digital signal generated by the analog-to-digital converter and the corresponding addresses of the linear digital values stored within the memory. Once corresponding addresses for the linear digital values are stored within the memory, the programming stage is removed and the serially coupled analog-to-digital converter and memory will reliably provide a greater degree of linearity between the analog signals applied to the converter and the digital values emanating from the memory.

Brief Description of the Drawings

[0012] A more complete appreciation of the inventions, and many of the attendant advantages thereof, will be readily enjoyed as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like numbers indicate the same or similar components, wherein:

[0013] Figure 1 is a schematic block diagram of a conventional application of an analog-to-digital converter.

[0014] Figure 2 is a schematic block diagram of an analog-to-digital converter circuit constructed according to the principles of the currently disclosed invention.

[0015] Figure 3 is a graphical representation of a ten step IRE staircase signal.

[0016] Figure 4 is a two coordinate graphical illustration of deviations in the degree of linearity occurring in a representative commercially available analog-to-digital converter.

[0017] Figure 5 is a two coordinate graphical illustration of one implementation of a process for performing analog-to-digital conversion according to the principles of the currently disclosed invention.

[0018] Figure 6 is a two coordinate graphical illustration of actual and theoretical responses obtained with one embodiments constructed according to the principles of the currently disclosed invention.

[0019] Figures 7A, 7B and 7C are two coordinate graphical illustrations providing expanded presentation of the detail of adjoining sections of the values illustrated in the graphical representation of Figure 6.

Detailed Description of the Invention

[0020] Referring now to Figure 1, a schematic illustration of a representative conventional digital signal processing system is shown. Such systems usually have an analog-to-digital converter as an input link from the analog domain. In the system of Figure 1, an analog signal is applied to an input port of an input circuit 10 which includes a gain adjustment stage, a direct current offset adjustment stage, and a clamp. The analog clock V_c transmitted by input circuit 10 is applied to an input port of an analog-to-digital converter 12 controlled by a sampling clock V_c, to provide digital data V_d on an "N" bit data bus 14 to a digital data processing system DSP 20. Referring now to Figure 4, a comparison of the uncorrected digital data V_d generated by converter 12 against the straight-line labelled "true linear" A/D converter output, shows that the digital data V_d deviate almost continuously over the range of conversion of converter 12, from a desired true linear relation between the A/D input analog signal V_i applied to the input port of converter 12 and the digital data V_d generated by converter 12.

[0021] A very simple circuit for linearizing analog-to-digital output according to the principles of the current invention, is illustrated in Figure 2. As was shown in Figure 1, the analog signal V_i transmitted by input circuit 10 is applied to an input port of an analog-to-digital converter 12 controlled by a sampling clock signal V_c, to provide digital data V_d on an "N" bit data bus 14.

[0022] An analog-to-digital linearizing memory 16, such as, for example, a programmable read-only-memory (i.e., a "PROM") storing a look-up table of digital values, is coupled to bus 14 to receive the digital data V_d, and to respond to the digital data V_d by providing true linear digital values from the look-up table to digital data processing system DSP 20 via an "N" bit data bus 18.

[0023] A microprocessor 22 may be temporarily coupled between the output port of converter 12 and the input port of memory 16 via bus 14, to serve as a switch between bus 14 and a programming memory 24 containing a table of true linear digital values V_t.

[0024] A known test signal such as a ten step IRE staircase signal, as shown in Figure 3, may be used as the analog input signal applied to input circuit 10. In such an instance, the true linear digital values V_t stored in programming memory 24 provide an accurate and reliable relation to a characteristic such as the amplitude of each step of the known test signal over the entire range of the known test signal. An IRE zone shown along the abscissa of the graph in Figure

3, is defined as an output range between the levels captured from the test signal. A, and B of Fig.5 are analog-to-digital output values delimiting the Kth zone for input level or interval between V_k and V_{k+1}. A_T, an B_T are corresponding correct (true linear) values for that zone. Then, a corrected value Y_T for the digital value Y of the non-linear A/D may be computed as:

$$Y_T = A_T + [(B_T - A_T)] * [(y-A)\div(B-A)] \quad (1)$$

$$= [A_T - [(B_T - A_T)\div(B-A)] * A] + [(B_T - A_T)\div(B-A)] * y \quad (2)$$

$$= C_k + D_k * y \quad (3)$$

where C_k and D_k are the parameters computed for the K_{th} zone from its measured values of A and B for a given A/D device with corresponding theoretical analog-to-digital output values of A_T and B_T.

[0025] The analog-to-digital output that results from a known test signal such as a ten step IRE staircase signal, is gated to microprocessor 22, for example, for a nine bit analog-to-digital converter 12, after basic gain and direct current offset are adjusted within input circuit 10 for a 0 to +1 V_{pp} signal input. The analog-to-digital output digital value will therefore range by 2^N, with N = 9, from -256 to +255 in offset two's complement. Microprocessor 22 obtains true digital values V_t from the look-up table stored within programming memory 24, for the known IRE levels. Correct digital values for each of these levels of amplitude of the IRE staircase test signal are known for the designated analog-to-digital device, and are stored within a look-up table within programming memory 24. In response to application of each of the levels of the IRE staircase test signal to input circuit 10, microprocessor 22 reads the corresponding true digital value V_t from programming memory 24 and stores that true digital value within the look-up table of linearizing memory 16, the corresponding true digital value, with the address of each of the true digital values stored within linearizing memory 16 being the corresponding uncorrected digital data V_d generated by converter 12. A microprocessor 22 is programmed to determine values between steps of an input signal analytically, as shown in Figure 5 for the step of V_k to V_{k+1}. After all of the true digital values over the range of converter 12 are stored within the look-up table of linearizing memory 16 at address corresponding to the values of digital data V_d generated by converter 12 in response to input of each of the levels of the known test signal, microprocessor 22 and programming memory 24 are removed and a linear analog-to-digital converter including input circuit 10, converter 12 and linearizing memory 16 are able to accurately generate digital values V_o exhibiting a true linear relation with a characteristic, such as amplitude, of an input analog signal V_i, over the entire range of converter 12. Thus, the input-to-output non-linearity intrinsic to a mass production quality analog-to-digital converter 12 can be reliably and inexpensively eliminated, or greatly reduced, simply by generating appropriate mapping via a read only memory (i.e., a "ROM") 16.

[0026] The plots illustrated in Figures 6, 7A, 7B and 7C were made for a TRW nine bit analog-to-digital converter evaluation board, Model No. TDC 1020 E1C. Figure 6 provides a two coordinate graphical illustration of actual and theoretical responses obtained with one embodiments constructed according to the foregoing principles currently disclosed, while figures 7A, 7B and 7C shown enlarged two coordinate graphical illustrations providing expanded presentation of the detail of adjoining sections of the values illustrated in the graphical representation of Figure 6. The plots of Figures 6, 7A, 7B and 7C show analog-to-digital output V_o (as dashed lines) and corrected values (as solid lines) using above described concept. The expanded views clearly depict that the nonlinearity can be practically eliminated over the entire digitizing range.

Claims

1. An analog-to-digital converter, comprising :

converter means (12) for converting amplitudes of a plurality of successive samples of an analog signal into first digital values representative of the amplitudes of said successive samples , said converting means being of a substantially linear type, in which the first digital values deviate from a desired true linear relation and storage means (16) for storing a plurality of second digital values at a plurality of distinct addresses, each one of said distinct addresses corresponding to a specific one of said plurality of first digital values, said plurality of second digital values extending over a range and exhibiting a true linear relation over said range to said amplitudes of said analog signal, and for responding to reception of said first digital values by outputting said

second digital values stored at corresponding ones of said plurality of distinct address,

characterized in that it further comprises:

means for applying during at least one selected time to said converter means (12) as said analog signal a test signal successively exhibiting values of said amplitude corresponding to said specific ones of said plurality of second digital values ;

means (24) for providing for each successively exhibited value of said amplitude in said test signal a corresponding one of said plurality of second digital values ; and

means (22) operable during each said selected time for writing said plurality of second digital values into said storage means (16) at addresses corresponding to said first digital values.

2. The converter of claim 1 wherein at times other than said selected times said converter means (12) responds to the amplitude of said analog signal by converting successive samples of said amplitude into digital words, each having one of said first digital values.

3. A method for linearizing an analog-to-digital converter responding to an analog input signal applied thereto to generate a digital output signal substantially linearly related to said analog input signal, said method using a random access memory, characterized by the steps of:

initially, in a procedure to write said random access memory simultaneously

supplying a prescribed test signal comprising successive samples of differing levels directly to said analog-to-digital converter as said analog input signal thereto,

supplying to said random access memory as write input data a digital number linearly related to the level of each sample currently supplied to said analog-to-digital converter as said analog input signal thereto, and

conditioning said random access memory to store write input data supplied thereto at locations addressed by the digital output signals of said analog-to-digital converter generated responsive to the successive samples of differing levels in said prescribed test signal, while

addressing said random access memory with the digital output signal of said analog-to-digital converter; and

thereafter, in a procedure to read from said random access memory a linearized digital response to an analog input signal other than said prescribed test signal,

supplying said other analog input signal to said analog-to-digital converter, and

conditioning said random access memory to read the contents stored in addressed said locations thereof, while

continuing to address said random access memory with the digital output signal of said analog-to-digital converter.

Patentansprüche

1. Analog-Digital-Wandler, enthaltend:

eine Wandlereinrichtung (12) zum Umwandeln der Amplituden mehrerer aufeinanderfolgender Tastwerte eines Analogsignals in erste Digitalwerte, die für die Amplituden der aufeinanderfolgenden Abschnitte repräsentativ sind, wobei die Wandlereinrichtung ein im wesentlichen linearer Typ ist, in dem die ersten Digitalwerte von einer gewünschten, echte linearen Beziehung abweichen, und

eine Speichereinrichtung (16) zum Speichern mehrerer zweiter Digitalwerte in mehreren bestimmten Adressen, wobei jede der bestimmten Adressen einem bestimmten aus der Vielzahl der ersten Digitalwerte ent-

spricht und sich die Vielzahl der zweiten Digitalwerte über einen Bereich erstreckt und eine tatsächlich lineare Beziehung über diesen Bereich zu den Amplituden des Analogsignals darstellt, und zum Antworten auf den Empfang der ersten Digitalwerte durch Ausgeben der zweiten Digitalwerte, die an entsprechenden Adressen aus der Vielzahl der bestimmten Adressen gespeichert sind, dadurch gekennzeichnet, daß er weiterhin enthält:

Einrichtungen, um während wenigstens einer ausgewählten Zeit der Wandlereinrichtung (12) als Analogsignal ein Testsignal zuzuführen, das nacheinander Werte der Amplitude darstellt, die den spezifischen Werten aus der Vielzahl der zweiten Digitalwerte entsprechen;

Einrichtungen (24), um für jeden nacheinander dargestellten Wert der Amplitude im Testsignal einen entsprechenden Wert aus der Vielzahl der zweiten Digitalwerte zu erzeugen; und

Einrichtungen (22), die während jeder ausgewählten Zeit betriebsbereit sind, um die Vielzahl zweiter Digitalwerte in die Speichereinrichtungen (16) in Adressen zu schreiben, die den ersten Digitalwerten entsprechen.

2. Wandler nach Anspruch 1, bei dem zu Zeiten, die sich von den gewählten Zeiten unterscheiden, die Wandlereinrichtung (12) auf die Amplitude des Analogsignals durch Umwandeln aufeinanderfolgender Tastwerte der Amplitude in digitale Worte antwortet, von denen jedes einen der ersten Digitalwerte aufweist.

3. Verfahren zum Linearisieren eines Analog-Digital-Wandlers, der auf ein ihm zugeführtes Analog-Eingangssignal antwortet, um ein Digital-Ausgangssignal zu erzeugen, das im wesentlichen linear auf das Analog-Eingangssignal bezogen ist, wobei bei diesem Verfahren ein RAM verwendet wird, gekennzeichnet, durch folgende Schritte:

zu Beginn in einem Vorgang zum gleichzeitigen Einschreiben in den RAM

Zuführen eines vorgeschriebenen Testsignals, das aufeinanderfolgende Tastwerte unterschiedlicher Pegel enthält, direkt zum Analog-Digital-Wandler als Analog-Eingangssignal,

Zuführen zum RAM als Schreibeingangsdaten einer Digitalzahl, die linear auf den Pegel jedes Tastwertes bezogen ist, der momentan dem Analog-Digital-Wandler zugeführt wird, als das Analog-Eingangssignal zum RAM, und

Einrichten des RAM, um Schreib-Eingangsdaten zu speichern, die diesem zugeführt werden, an Bereichen, die durch die Digital-Ausgangssignale des Analog-Digital-Wandlers adressiert sind und in Abhängigkeit der aufeinanderfolgenden Tastwerte unterschiedlicher Pegel im vorgeschriebenen Testsignal erzeugt werden, während

der RAM mit dem Digital-Ausgangssignal des Analog-Digital-Wandlers adressiert wird; und

anschließend in einem Vorgang zum Lesen aus dem RAM einer linearisierten Digitalantwort auf ein Analog-Eingangssignal, das sich vom vorgeschriebenen Testsignal unterscheidet,

Zuführen des anderen Analog-Eingangssignals zum Analog-Digital-Wandler, und

Einrichten des RAM zum Lesen der Inhalte, die an seinen adressierten Stellen gespeichert sind, während

mit der Adressierung des RAM mit dem Digital-Ausgangssignal des Analog-Digital-Wandlers fortgefahren wird.

Revendications

1. Convertisseur analogique-numérique, comprenant :

- des moyens de conversion (12) pour convertir des amplitudes d'une pluralité d'échantillons successifs d'un signal analogique en premières valeurs numériques représentatives des amplitudes desdits échantillons successifs, lesdits moyens de conversion étant d'un type sensiblement linéaire, dans lequel les premières valeurs numériques s'écartent d'une relation linéaire vraie souhaitée; et
- des moyens de stockage (16) pour stocker une pluralité de deuxièmes valeurs numériques à une pluralité

d'adresses distinctes, chacune desdites adresses distinctes correspondant à une valeur spécifique de ladite pluralité de premières valeurs numériques, ladite pluralité de deuxièmes valeurs numériques s'étendant sur une gamme et représentant une relation linéaire vraie sur ladite gamme par rapport auxdites amplitudes dudit signal analogique, et pour répondre à la réception desdites premières valeurs numériques en sortant lesdites deuxièmes valeurs numériques stockées à des adresses correspondantes de ladite pluralité d'adresses distinctes,

caractérisé en ce qu'il comprend en outre :

- des moyens pour appliquer pendant au moins un instant sélectionné, auxdits moyens de conversion (12), en tant que dit signal analogique, un signal de test présentant successivement des valeurs de ladite amplitude correspondant auxdites valeurs spécifiques de ladite pluralité de deuxièmes valeurs numériques;
- des moyens (24) pour fournir, pour chaque valeur présentée successivement de ladite amplitude dans ledit signal de test, une valeur correspondante de ladite pluralité de deuxièmes valeurs numériques; et
- des moyens (22), opérationnels pendant chaque instant sélectionné, pour écrire ladite pluralité de deuxièmes valeurs numériques dans lesdits moyens de stockage (16) à des adresses correspondant auxdites premières valeurs numériques.

2. Convertisseur selon la revendication 1, dans lequel à des instants autres que lesdits instants sélectionnés lesdits moyens de conversion (12) répondent à l'amplitude dudit signal analogique en convertissant des échantillons successifs de ladite amplitude en mots numériques, chacun ayant une desdites premières valeurs numériques.

3. Procédé pour linéariser un convertisseur analogique-numérique répondant à un signal d'entrée analogique appliqué à celui-ci, pour générer un signal de sortie numérique sensiblement en rapport linéaire avec ledit signal d'entrée analogique, ledit procédé utilisant une mémoire à accès aléatoire, caractérisé par les étapes de :

- initialement, dans une procédure pour écrire ladite mémoire à accès aléatoire, et simultanément
  - -- fourniture d'un signal de test prescrit, comprenant des échantillons successifs de niveaux différents, directement audit convertisseur analogique-numérique en tant que dit signal d'entrée analogique de celui-ci,
  - -- fourniture à ladite mémoire à accès aléatoire, en tant que donnée d'entrée d'écriture, d'un nombre numérique en rapport linéaire avec le niveau de chaque échantillon actuellement fourni audit convertisseur analogique-numérique en tant que dit signal d'entrée analogique de celui-ci, et
  - -- conditionnement de ladite mémoire à accès aléatoire pour stocker des données d'entrée d'écriture fournies à celle-ci à des emplacements adressés par les signaux de sortie numériques dudit convertisseur analogique-numérique générés en réponse aux échantillons successifs de niveaux différents dans ledit signal de test prescrit, pendant
  - -- l'adressage de ladite mémoire à accès aléatoire avec le signal de sortie numérique dudit convertisseur analogique-numérique; et
- par la suite, dans une procédure pour lire depuis ladite mémoire à accès aléatoire une réponse numérique linéarisée à un signal d'entrée analogique autre que ledit signal de test prescrit :
  - -- fourniture dudit autre signal d'entrée analogique audit convertisseur analogique-numérique, et
  - -- conditionnement de ladite mémoire à accès aléatoire pour lire le contenu stocké dans lesdits emplacements adressés de celle-ci, pendant
  - -- la continuation de l'adressage de ladite mémoire à accès aléatoire avec le signal de sortie numérique dudit convertisseur analogique-numérique.

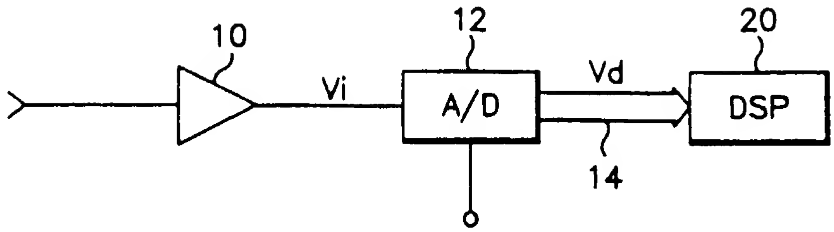


FIG. 1

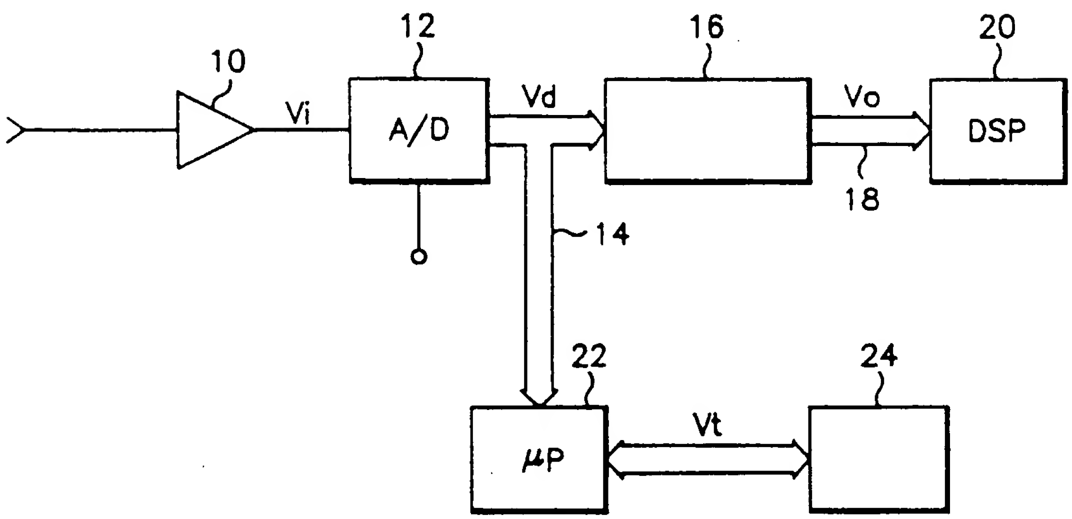
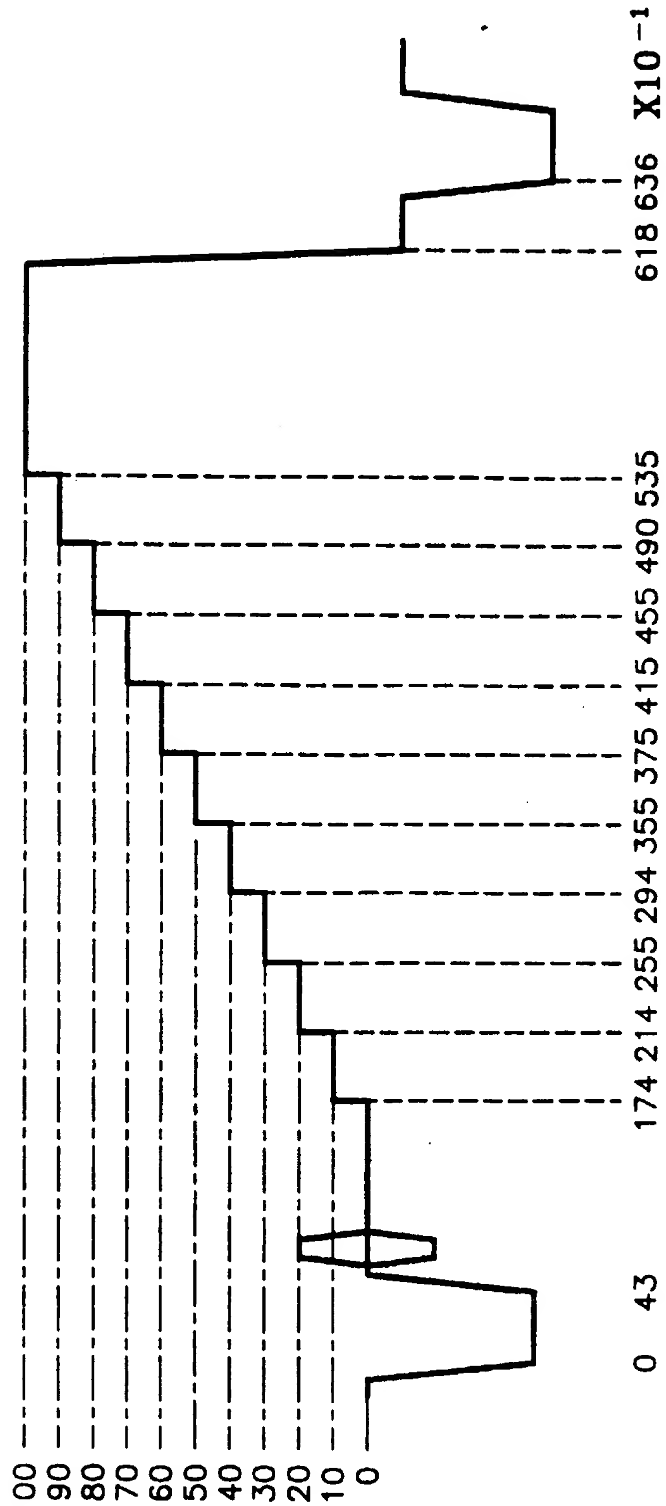


FIG. 2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30
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490
535
618
636
X10 -1

FIG. 3

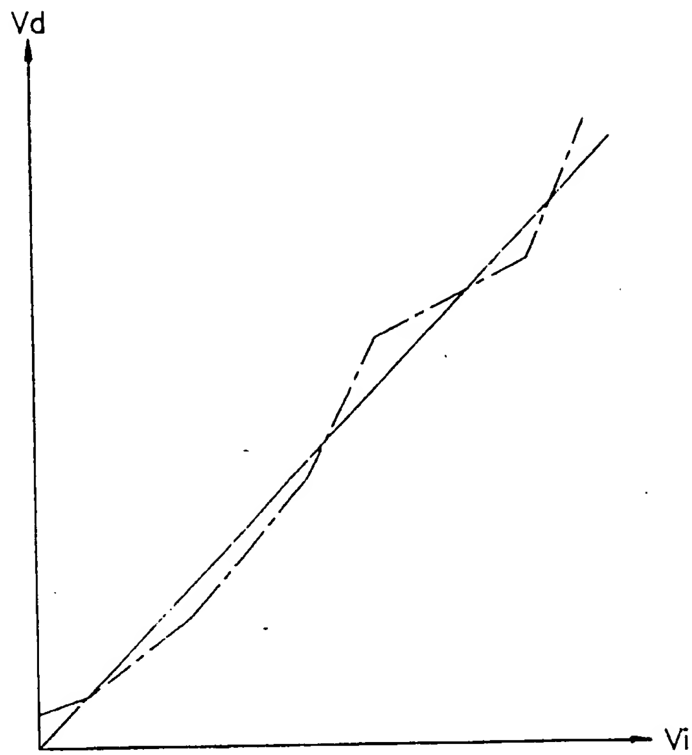
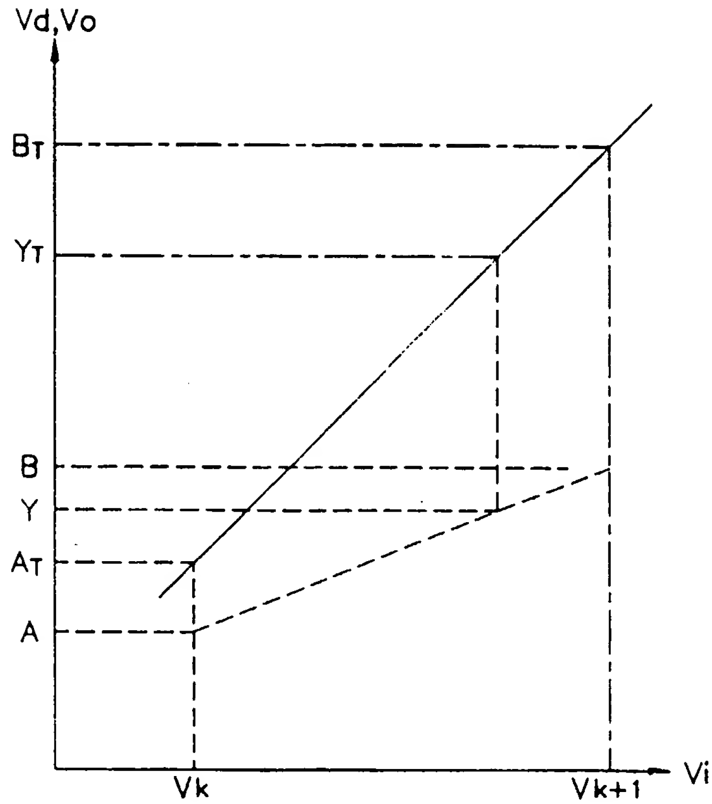
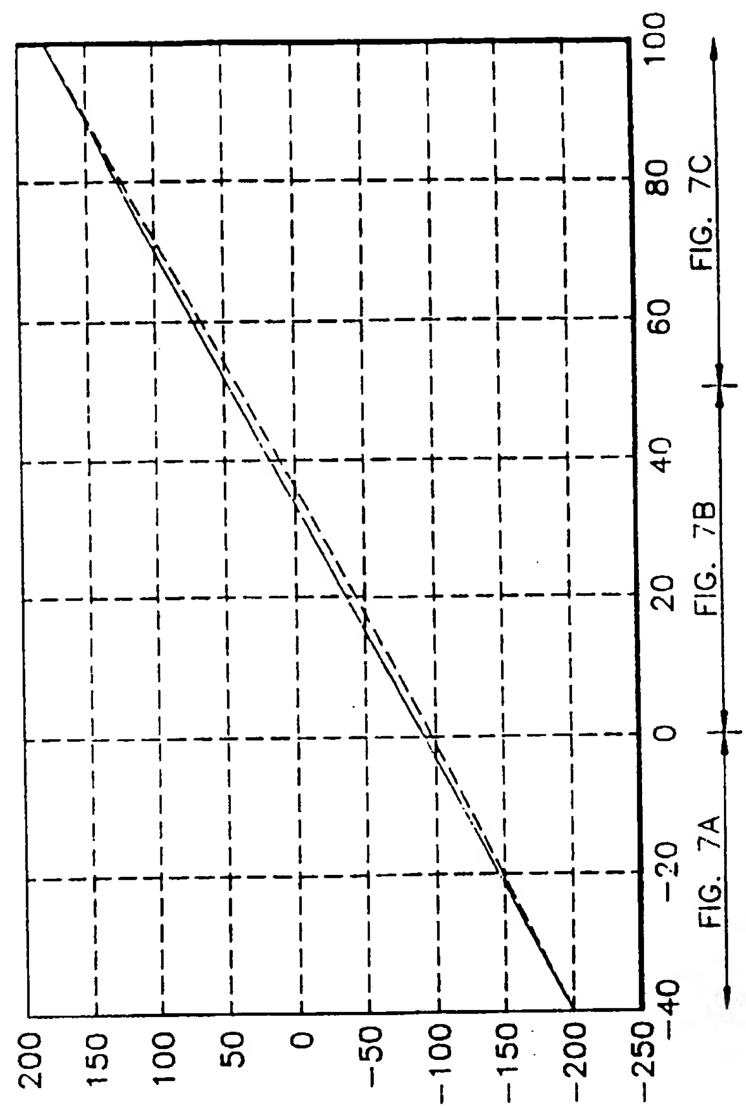


FIG. 4



$$Y_T = A_T + \frac{(Y-A)}{(B-A)} \cdot (B_T - A_T)$$

FIG. 5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−50
−100
−150
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−20
0
20
40
60
80
100
FIG. 7A
FIG. 7B
FIG. 7C

FIG. 6

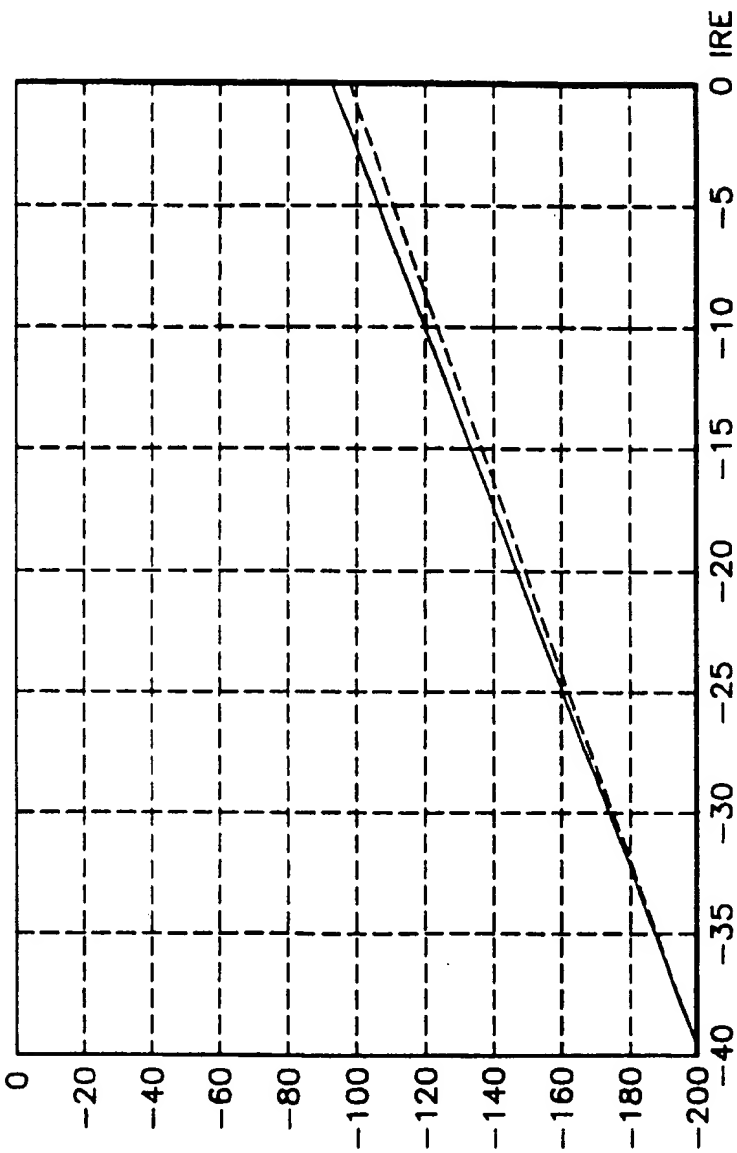
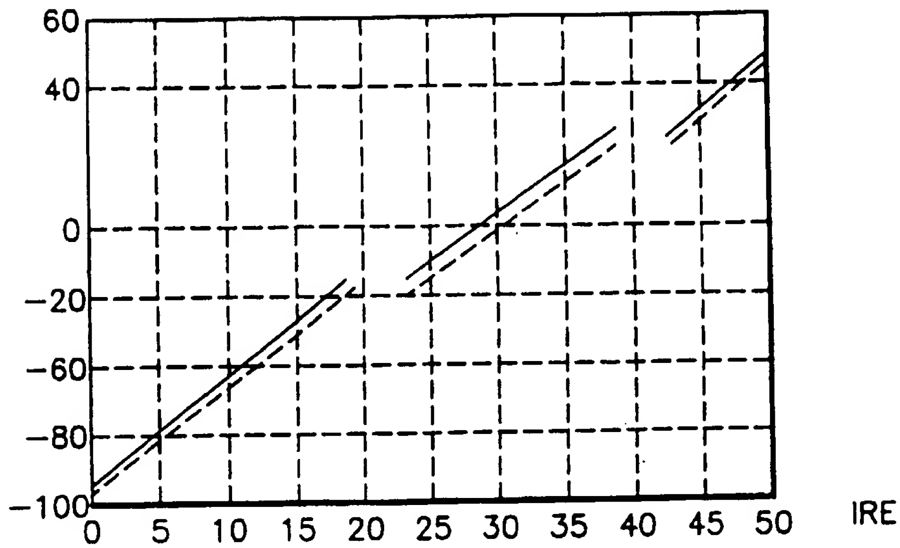


FIG. 7A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−60
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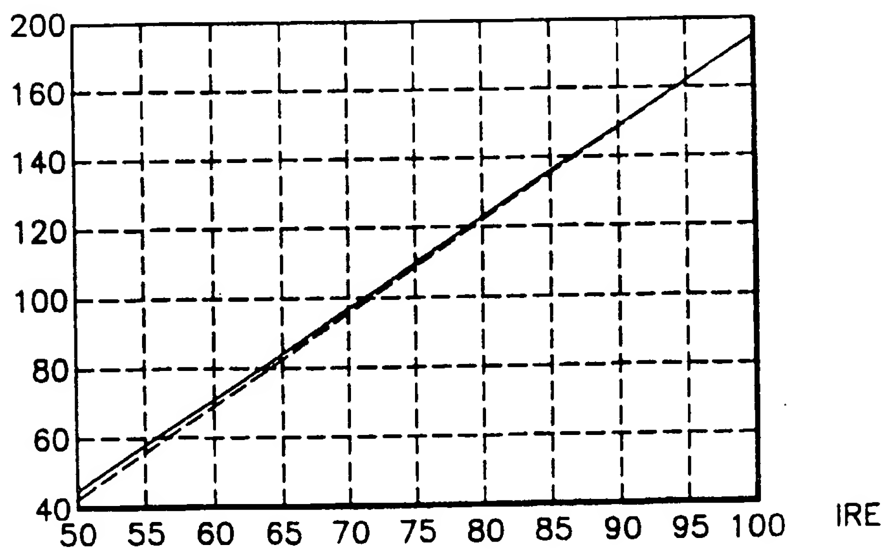
−100
0 5 10 15 20 25 30 35 40 45 50
IRE

FIG. 7B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140
120
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80
60
40
50 55 60 65 70 75 80 85 90 95 100
IRE

FIG. 7C